WHAT IS CLAIMED IS:

1. A semiconductor device, the semiconductor device comprising a semiconductor substrate, wherein the semiconductor substrate has on its top at least a Thin Strain Relaxed Buffer consisting essentially of a stack of three layers, wherein the Thin Strain Relaxed Buffer is not an active part of the semiconductor device, and wherein the three layers have a substantially constant Ge concentration, the three layers comprising:

a first epitaxial layer of $Si_{1-x}Ge_x$, wherein x is the Ge concentration;

a second epitaxial layer of $Si_{1-x}Ge_x$: C on the first epitaxial layer, wherein a C concentration in the second epitaxial layer is greater than or equal to about 0.3 %; and

a third epitaxial layer of $Si_{1-x}Ge_x$ on the second epitaxial layer.

2. The semiconductor device of Claim 1, wherein the semiconductor substrate comprises silicon.

3. The semiconductor device of Claim 1, wherein a thickness of the second epitaxial layer is from about 1 nm to about 20 nm.

4. The semiconductor device of Claim 1, wherein a thickness of the second epitaxial layer is from about 1 nm to about 10 nm.

5. The semiconductor device of Claim 1, wherein a thickness of the second epitaxial layer is about 5 nm.

6. The semiconductor device of Claim 1, wherein the Ge concentration is from about 5 % to about 100 %.

7. The semiconductor device of Claim 1, wherein the Ge concentration is from about 10 % to about 65 %.

8. The semiconductor device of Claim 1, wherein the C concentration is from about 0.5 % to about 1 %.

9. The semiconductor device of Claim 1, wherein the C concentration is about 0.8%.

10. The semiconductor device of Claim 1, further comprising a SiGe/Si heterostructure at the top of the Thin Strain Relaxed Buffer, the heterostructure comprising a strain adjusted SiGe layer and a strained Silicon layer.

11. The semiconductor device of Claim 1, further comprising a III-V compound at its top.

12. The semiconductor device of Claim 1, further comprising an additional epitaxial $Si_{1-x}Ge_x$:C layer underneath the first epitaxial SiGe layer.

13. The semiconductor device of Claim 12, further comprising an additional epitaxial $Si_{1-x}Ge_x$ underneath the additional epitaxial $Si_{1-x}Ge_x$:C layer.

14. A method for growing a Thin Strain Relaxed Buffer, the method comprising:

providing a semiconductor substrate;

depositing a first SiGe epitaxial layer on at least a part of the semiconductor substrate such that the Ge concentration is substantially constant throughout the first epitaxial layer;

depositing a second SiGe:C layer on top of the first SiGe epitaxial layer by growing SiGe comprising at least 0.3 % carbon such that the Ge concentration is substantially constant throughout the SiGe:C layer and substantially the same as in the first layer; and

depositing a second SiGe epitaxial layer on top of the SiGe:C layer, wherein the Ge concentration is substantially constant throughout the third layer.

15. The method according to Claim 14, wherein the semiconductor substrate comprises silicon.

16. The method according to Claim 14, wherein the Ge concentration is from about 5 % to about 100 %.

17. The method according to Claim 14, wherein the Ge concentration is from about 10 % to about 65%.

18. The method according to Claim 14, wherein the C concentration is from about 0.5 % to about 1 %.

19. The method according to Claim 14, wherein the C concentration is about 0.8%.

20. The method according to Claim 14, further comprising:

providing a first precursor gas and a second precursor gas, wherein the first precursor gas comprises a Si containing compound or a compound of formula

SiH_zCl_w, wherein z and w are independently from 1 to 4, wherein the second precursor gas comprises a Ge bearing precursor compound, wherein the layers are deposited making use of the first precursor gas and the second precursor gas.

21. The method according to Claim 14, further comprising:

providing a carbon containing gas, wherein the carbon containing gas comprises a C bearing compound.

22. The method according to Claim 14, further comprising:

depositing an additional epitaxial $Si_{1-x}Ge_x$:C layer underneath the first epitaxial SiGe layer on at least a part of the semiconducting substrate.

23. The method according to Claim 22, further comprising:

depositing an additional epitaxial $Si_{1-x}Ge_x$ layer underneath the additional epitaxial $Si_{1-x}Ge_x$:C layer on at least a part of the semiconducting substrate.

24. The method according to Claim 14, further comprising:

depositing an additional silicon cap layer on top of the third epitaxial layer.

25. The method according to Claim 14, further comprising:

exposing a structure comprising the semiconductor substrate and the three epitaxial layers to a temperature of 800°C or higher, whereby a maximum temperature is defined by a melting point of the SiGe layer.

26. The method according to Claim 25, wherein the structure further comprises at least one of the additional layers.

27. The method according to Claim 14, further comprising:

depositing a strain adjusted SiGe layer on top of a Thin Strain Relaxed Buffer.

28. The method according to Claim 27, further comprising:

depositing a strained silicon layer on top of the strain adjusted SiGe layer.

29. The method according to Claim 25, wherein depositing the three epitaxial layers and exposing to a temperature of 800°C or higher are performed without exposure to an oxidizing atmosphere in between depositing and exposing.

30. The method according to Claim 24, wherein depositing the three epitaxial layers and depositing the additional silicon cap layer are performed without exposure to an oxidizing atmosphere in between depositing.

31. The method according to Claim 25, further comprising depositing an additional silicon cap layer on top of the third epitaxial layer, wherein exposing and depositing are performed without exposure to an oxidizing atmosphere in between.

32. The method according to Claim 14, wherein the method is performed without exposure to an oxidizing atmosphere between depositing layers.

33. The method according to Claim 14, wherein the method is performed in a same tool without exposure to an oxidizing atmosphere in between depositing layers.

34. The method according to Claim 14, wherein the substrate is a blanket wafer.

35. The method according to Claim 14, wherein the substrate is a patterned wafer.